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-	2	("6166961").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:32
-	11614	negative near10 pump$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:39
-	12860	eras$3 near5 (voltage$1 or potential)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:47
-	53321	read$3 near5 (voltage$1 or potential)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:48
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-	449909	driver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:52
-	73809	365/$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/02 12:54
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-	7168	level adj shifter$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 09:45
-	2623	negative adj3 pump$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 09:47
-	12772	positive adj3 pump$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 09:50
-	249554	(block$1 or bank$1) near5 control$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 10:22
-	73956	365/$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 10:25
-	2	(level adj shifter$1) and (negative adj3 pump$1) and (positive adj3 pump$1) and ((block$1 or bank$1) near5 control$4) and 365/$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/08 10:25

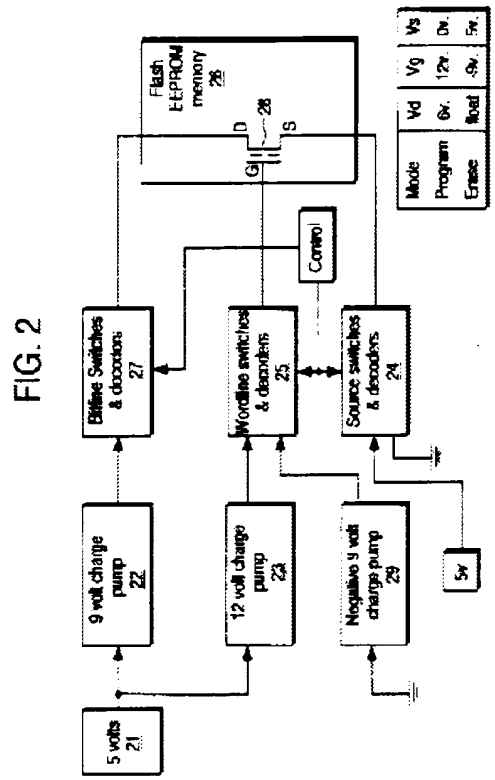

FIG. 2

(12) **United States Patent**
Rao

(10) **Patent No.: US 6,359,947 B1**
(45) **Date of Patent: Mar. 19, 2002**

(54) **SPLIT CLOCK BUFFERS FOR A NEGATIVE CHARGE PUMP**

(75) Inventor: **Hari M. Rao**, Fair Oaks, CA (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/387,641**

(22) Filed: **Aug. 31, 1999**

(51) Int. Cl.[7] H03D 3/24

(52) U.S. Cl. 375/374, 327/536

(58) Field of Search 375/374, 327/536, 327/530, 305; 365/226, 218, 149

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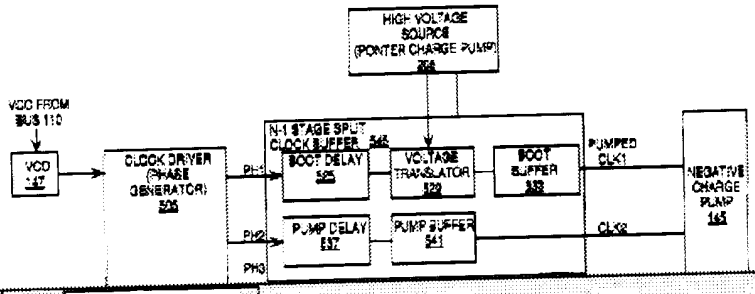
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

A split clock buffer for providing clock signals to a negative charge pump. The split clock buffer receives a first phase and a second phase of the clock signal, pumps the voltage level of the first phase from a first voltage level to a second voltage level. Then, the buffer outputs the pumped first phase to a boot node of the negative charge pump, and outputs the second phase to a pump node of the negative charge pump.

37 Claims, 12 Drawing Sheets



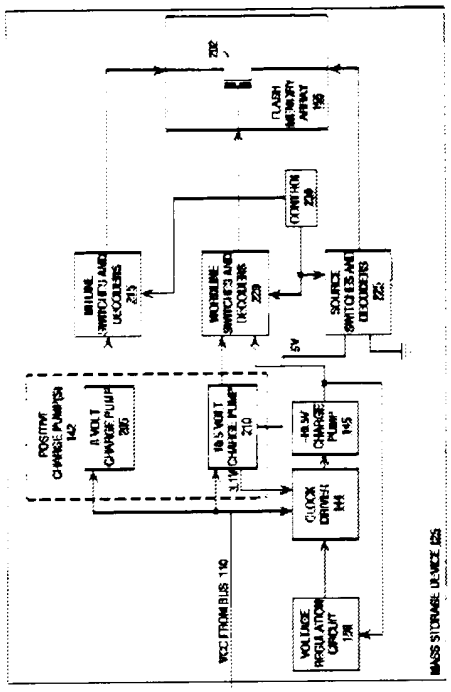
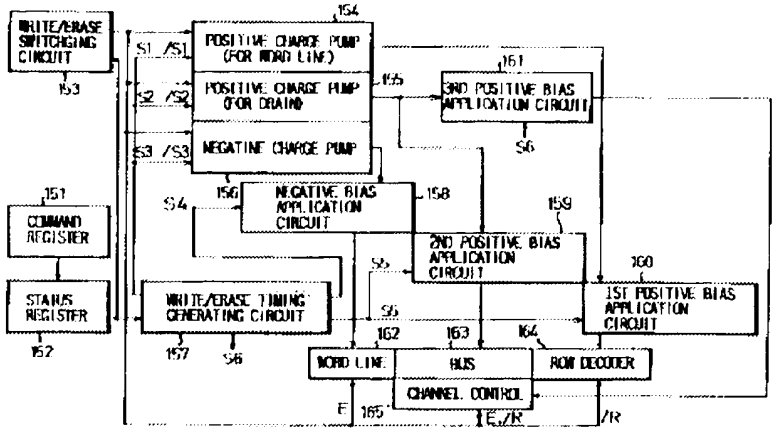


FIG. 2

Fig.9



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10	☐	☐	US 5406524 A	19950411	41	Nonvolatile semiconductor memory that eases the	365/185.27	365/185.1; 365/185.18;	

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